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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/670,352	09/26/2003	Tomohiro Taira	501.41197CX1	5276

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EXAMINER	
STEVENSON, ANDRE C	

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 02/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/670,352	TAIRA, TOMOHIRO .	
	Examin r	Art Unit	
	Andre' C. Stevenson	2812	

-- The MAILING DATE of this communicati n appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 9/26/03.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-9 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-9 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 26 September 2003 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 10/096,801.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Lynne A. Burley

LYNNE A. URLEY
PRIMARY PATENT EXAMINER
TC 2800, AU 2812

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 09/26/03.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Foreign Priority

Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d). The certified copy has been filed in parent Application No. 10096801, filed on March 14, 2002.

Objections to Claims

Claim 9 is objected to because of the following informalities: Claim 9 fails to have a period at the end of the sentence. Also, it cannot be concluded if this is all Applicant was intended to claim, or if there are further additions to the claim that were omitted. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1 through 9 are rejected under 35 U.S.C. 102(b) as being anticipated by Anderson (U.S. Pat 5,834,838, Patented Date November 10 1998, Filing Date December 19, 1996).

Anderson teaches, with respect to claim 1, a method of fabricating a semiconductor integrated circuit device, comprising the steps of: (a) performing a wafer process to a plurality of wafers, thereby forming a plurality of semiconductor integrated circuit devices over each of the wafers (Fig. 1, Column 5, lines 42 through 65); (b) after step (a), performing a first electrical test to a first set of wafers selected from the plurality of wafers accommodated in a first wafer cassette placed in a wafer prober (Fig.2, Column 5, lines 65 through 67; Column 6, lines 1 through 12; Column 14, lines 12 through 24); and (c) after step (a), performing a second electrical test to a second set of wafers selected from the plurality of wafers accommodated in a second wafer cassette placed in the wafer prober by automatically changing a test object to the second set of wafers (Column 15, lines 64 through 67; Column 16, lines 1 through 12).

Pertaining to **Claim #2**, Anderson teaches the method according to claim 1, wherein the first electrical test and the second electrical test are substantially the same test. Specifically, in column 6, line 62 through 64, Anderson states that "an incoming inspection operation is often performed on each lot of wafers"(column 1, lines 57 through 67; column 2, lines 1 through 3; column 3, lines 1 through 20; column 5, lines 40 through 67; column 6, lines 1 through 32, lines 64-67; column 7, lines 50 through 60; column 9, lines 60 through 67; column 10, lines 1 through 3). The examiner takes the position that this inspection operation and the tests which follow, are substantially the same for each lot of wafers.

Pertaining to **Claim #3**, Anderson teaches the method according to claim 2, wherein the first wafer set and the second wafer set are substantially the same product typed wafers (column 3, lines 20 through 67; column 4, lines 1 through 8; column 5, lines 65 through 67; column 6, lines 1 through 22; column 7, lines 50 through 59; column 9, lines 60 through 67; column 10, lines 1 through 3).

Anderson teaches, with respect to **Claim #4**, a method of fabricating a semiconductor integrated circuit device comprising the steps of: (a) performing a wafer process to a plurality of wafers, thereby forming a plurality of semiconductor integrated circuit devices over each of the wafers (Fig. 1, Column 5, lines 42 through 65), (b) after step (a), performing a first electrical test to a first set of wafers selected from the plurality of wafers accommodated in a first wafer cassette placed in a wafer prober (Fig.2, Column 5, lines 65 through 67; Column 6, lines 1 through 12; Column 14, lines 12 through 24), and (c) in step (b), performing checking of image data of probing needle traces of the wafer prober, (Column 10, lines 35 through 65). The examiner notes that "performing checking of image data of probing needle traces of the wafer prober" is not explicitly stated; however, the examiner considers that column 10, line 61-64, when compared to the claim and to applicants specifications (described on page 15, paragraph 10), satisfies the limitation as claimed by Applicant.

Pertaining to **Claim #5**, Anderson teaches the method according to claim 4, wherein in the step (b), a probing position of the wafer prober is corrected on the basis of the result of having checked the probe trace image data. (Column 10, lines 20 through 65).

Pertaining to **Claim #6**, Anderson teaches the method according to claim 5, wherein the electrical test is a probe check (Column 10, lines 35 through 65).

Pertaining to **Claim #7**, Anderson teaches a method of fabricating a semiconductor integrated circuit device, comprising the steps of: (a) performing a wafer process to a plurality of wafers, thereby forming a plurality of semiconductor integrated circuit devices over each of the wafers (Fig. 1, Column 5, lines 42 through 65), (b) after step (a), performing a first electrical test with a first test program to a first set of wafers selected from the plurality of wafers accommodated in a first wafer cassette placed in a wafer prober (Fig.2, Column 5, lines 65 through 67; Column 6, lines 1 through 12; Column 14, lines 12 through 24), and (c) after step (a), performing a second electrical test with a second test program to a second set of wafers selected from the plurality of wafers accommodated in a second wafer cassette placed in the wafer prober by automatically changing a test program from the first test program to the second test program (Fig.4, item 570, Column 14, lines 12 through 27; Column 15, lines 43 through 50).

Pertaining to **Claim #8**, Anderson teaches the method according to claim 7, wherein the second electrical test is performed by automatically changing a test object to the second set of wafers, (Column 23, lines 45 through 60; Column 15, lines 45 through 50; Column 19, lines 35 through 51).

Pertaining to **Claim #9**, Anderson teaches the method according to claim 8, wherein the electrical test is a probe. (Column 5, lines 65 through 67; Column 6, lines 1 through 12).

Conclusion

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866 – 217 – 9197 (toll-free).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andre C. Stevenson whose telephone number is (571) 272 1683. The examiner can normally be reached on Monday through Friday from 8:00 am to 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael S. Lebentritt, can be reached on 571-272-1873. The fax phone number for the organization where this application or proceeding is assigned is (703) 308 7724.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308 1782. Also, the proceeding numbers can be used to fax information through the Right Fax system;

- **703 872 9306**

Andre C. Stevenson

Art Unit 2812

1/18/05

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